Digitally assisted calibration of RF sampling ADCs

Towards co-optimization of circuit design and digitally assisted calibration

In the ever-evolving field of wireless communication, where speed and reliability are crucial, high-speed Analog-to-Digital Converters (ADCs) play a vital role. Future wireless communication standards demand ultra-high data rates, necessitating ADCs that operate at high sampling rates (>10 GS/s), offer high effective accuracy (>8 bits), and maintain high linearity. ADC designers face the challenge of balancing power consumption, bandwidth, and linearity requirements. As CMOS technologies continue to scale down, achieving high linearity becomes increasingly difficult due to the typically high power consumption associated with it.

There are two primary approaches to addressing this linearity challenge. The first involves innovative circuit-level and system-level designs to develop new ADC systems and architectures. The second approach relies on digital calibration to correct the ADC's non-ideal behavior. This PhD research will focus on combining circuit-level design with digital (non)linear calibration techniques to enhance ADC performance. The goal is to achieve co-optimization between circuit design and digitally assisted calibration, paving the way for more efficient and effective ADCs.

The objective of this PhD research is to pioneer calibration techniques tailored for contemporary high-speed ADCs and contribute to the design of RF sampling ADCs. These correction algorithms must be executed directly on the chip, imposing unique constraints that make the research both interesting and challenging. The initial phase of the PhD program will involve proposing candidate models to rectify the non-ideal characteristics of the ADC. You will begin by designing an RF sampling ADC in an advanced CMOS technology . The resulting circuit and system-level simulations will guide the nonlinear calibration technique. The proposed models should also be suitable for efficient implementation in Digital Signal Processing (DSP) systems, with system identification algorithms formulated and applied. The combination of the chosen model and identification algorithm will provide the specifications needed to establish a comprehensive measurement setup. The lessons and constraints learned during this PhD will directly contribute to the co-development and design of the next generation of high-speed ADCs. You will collaborate with a team of expert designers eager to implement these algorithms to enhance the performance of their future designs.

This PhD aims to combine the expertise of IMEC and the Vrije Universiteit Brussel (VUB). At IMEC, you will join the team of Jan Craninckx and Piet Wambacq, one of the world-leading groups in high-performance RF, millimeter-wave and ADC design, with a strong publication record in the major conferences and journals of the solid-state circuits community. At the VUB, you will be embedded within the ELEC department, renowned for its expertise in nonlinear system identification and signal processing.

Required background: We are looking for excellent candidates that have a strong background in RF and analog IC design and preferably have some experience with high-frequency design, layout or measurement techniques, and characterization

Type of work: 10% literature, 20% circuit-level simulation, 30% design, 20% programming, 20% measurements
Supervisor: Piet Wambacq
Co-supervisor: Dries Peumans
Daily advisor: Adam Cooman, Nereo Markulic

Please contact Piet Wambacq (Piet.Wambacq@vub.be) for more information